

Abstract

Main-transistors M1 and M2 are divided into sub-transistors that are arrayed in a matrix with four rows and four columns to form four cells so that each of the cells is formed of
5 four of the sub-transistors that have a common center. This can realize a layout configuration that is as good in matching of the main-transistors M1 and M2 as a four-segment layout scheme and takes small pattern area.